Reducing the output harmonics and the number components in high frequency distribution system by using a switched-capacitor-based cascaded multilevel inverter

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Abstract: *The increase of frequency in AC transmission system has more advantages than low- or medium frequency distribution systems. In high-frequency ac Power Distribution System the high-Frequency inverter serves as source. Here the high frequency inverter is obtained with a switched-capacitor-based cascaded multilevel inverter is proposed in this work. The inverter is constructed by a combination of switched-capacitor and H Bridge inverter. The the conversion of series and parallel connections, the switched capacitor increases the number of voltage levels in the output. The harmonics in the output and the number of components can be significantly reduced by the increasing number of voltage levels in the output waveform. The symmetrical triangular waveform modulation with analog implementation is used in this circuit topology. The mathematical analysis, determination of circuit parameters is examined. The computer simulation results confirm the feasibility of proposed multilevel inverter.*

Keywords: *Cascaded H-Bridge inverter, high-frequency ac, multilevel inverter, switched capacitor*

1. Introduction

In previous technique DC to AC conversion technique process the output has high amount of harmonics, in order to reduce this harmonics we develop a new project; in this a novel switched capacitor is introduced for the purpose in increase the voltage levels. In addition to this the H bridge also used. In this project we generate the gate pulses by using PWM technique. The switched capacitor situated at the front end and the H bride at back end. By using this project the harmonics are significantly reduced from high level to low level. In this project the efficiency of the out voltage is increased to certain level. To overcome the above problem of two methods we are going for cascaded multi level inverter based on switched capacitor for high frequency AC power distribution system. In this project we want to increase the levels of output voltage at any cost without problem discussed above. We used two cascaded H-Bridge inverters and capacitors which, used increase the output voltage more than input voltage. By using this total harmonics are reduced because of the increased levels in the output voltage.

High-Frequency AC Power Distribution System becomes an alternative to dc distribution due to the lesser components and lower cost. The present inverter applications can be found in computer, telecom, electric vehicle and renewable energy micro grid [[1],[2]. However high-frequency AC Power Distribution System has to confront the challenges from large power capacity, high Electromagnetic Interference, and severe power losses [3]. In order to increase the power capacity, the most popular method is to connect the inverter output in series or in parallel. However, it is impractical for high-frequency inverter, because it is complicated to simultaneously synchronize both amplitude and phase with high frequency dynamics. Multilevel inverter is an effective solution to increase power capacity without synchronization consideration, so the higher power capacity is easy to be achieved by multilevel inverter with lower switch stress. Non polluted sinusoidal waveform with the lower Total Harmonic Distortion (THD) is critically caused by long track distribution in HFAC PDS. The higher number of voltage levels can effectively decrease total harmonics content of staircase output, thus significantly simplifying the filter design [4]. HF power distribution is applicable for small-scale and internal closed electrical network in Electric vehicle (EV) due to moderate size of distribution network and effective weight reduction [5]. The consideration of operation frequency has to make compromise between the ac inductance and resistance [6], so multilevel inverter with the output frequency of about 25 kHz is a feasible trial to serve as power source for high-frequency EV application. The traditional topologies of multilevel inverter mainly are diode-clamped and capacitor-clamped type [7], [8]. In this project the efficiency of the out voltage is increased to certain level. To overcome the above problem of two methods we are going for cascaded multi level inverter based on switched capacitor for high frequency AC power distribution system. In this project we want to increase the levels of output voltage at any cost without problem discussed above. We used two cascaded H-Bridge inverters and capacitors which, used increase the output voltage more than input voltage. By using this total harmonics are reduced because of the increased levels in the output voltage.

2. Fault diagnosis in multilevel converters

Since a multilevel converter is normally used in medium to high power applications, the reliability of the multilevel converter system is very important. For instance industrial drive applications in manufacturing plants are dependent upon induction motors and their inverter systems for process control. Generally, the conventional protection systems are passive devices such as fuses, overload relays, and circuit breakers to protect the inverter systems and the induction motors. The protection devices will disconnect the power sources from the multilevel inverter system whenever a fault occurs, stopping the operated process. Downtime of manufacturing equipment can add up to be thousands or hundreds of thousands of dollars per hour, therefore fault detection and diagnosis is vital to a company's bottom line. In order to maintain continuous operation for a multilevel inverter system, knowledge of fault behaviors, fault prediction, and fault diagnosis are necessary. Faults should be detected as soon as possible after they occur, because if a motor drive runs continuously under abnormal conditions, the drive or motor may quickly fail.

3.Cascaded nine level inverter with nine-level output.

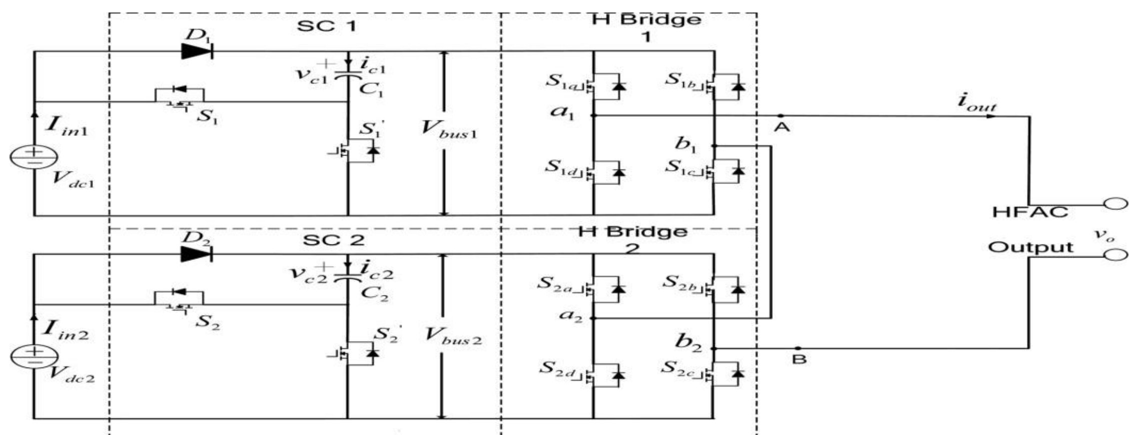

Fig .1 Nine Level Inverter for nine level output

The proposed circuit is made up of the switched capacitor and cascaded H-Bridge inverter. If the numbers of voltage levels obtained by switched capacitor and cascaded H-Bridge inverte are *N*1 and *N*2 , then the number of voltage levels is 2 ×*N*1×*N*2+1 in the entire operation cycle.Fig 1 shows the circuit topology of nine-level inverter (*N*1 =2, *N*2 = 2), where *S*1*, S*2*,* S^1 , S^2 as the switching devices of switched capacitor circuits (SC1 and SC2) are used to convert the series or parallel connection of *C*1 and *C*2 . *S*1*a, S*1*b, S*1*c, S*1*d, S*2*a, S*2*b, S*2*c, S*2*d*are the switching devices of cascaded H-Bridge. *Vdc*1 and *Vdc*2 are input voltage. *D*1 and *D*2 are diode to restrict the currents direction. I_{out} and *vo* are the output current and the output voltage, respectively.*Vc* is the triangular carrier, and *Vpp* is the peak value of *Vc*. The modulation signals of triangular carrier are *Vm* 1*c, Vm* 1*b, Vm* 2*c* and *Vm* 2*b* . *Vm* 1*b* and *Vm* 2*b* are used to control phase-shift angles of H-Bridge 1 and H-Bridge 2, respectively, and *δi* is the duration of voltage levels controlled by them. Vm 1c and Vm 2c are used to control the alternative operations of SC1 and SC2, respectively, and αi is the duration of voltage levels controlled by them. Thus, the drive signals of H-Bridge switches ($S1a$, $S1b$, $S1c$, $S1d$, $S2a$, $S2b$, $S2c$, $S2d$) are phase-shifted pulse signals, while the drive signals of SC switches ($S1$, $S2$, S_1 , S_2)are complementary pulse signals.

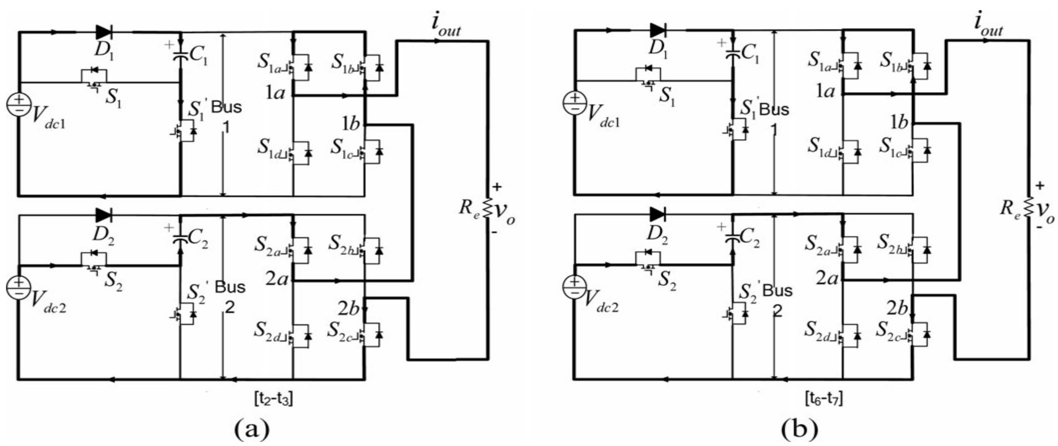

Fig . 2. Active circuits for different operation intervals in the operational modes

.The operations H-Bridge 1 is in freewheeling state, and H-Bridge 2 is in Fig. 2. Output voltage equals 2Vin because S1 and S2 are on, the capacitor C1 keeps charged to Vin and capacitor C2 is discharged. The voltages on Bus 1 and Bus 2 are Vin and 2Vin , respectively. The current flow of this time intervals shown in Fig(a). Similarly, the active circuit of $t6 \le t < t7$is shown in Fig (b) that has the same operations as $t2 \le t < t3$. The second half-cycle (from t8 on) has the similar active circuits as the first half-cycle ($t1 - t8$), but the current will be circulated in the opposite direction to provide the negative output voltage. The relations of on-state switches and output voltage level are described in Table I, as well as operations of two modes are compared closely. Table I has ten working states for nine voltage levels. When the operation enters a new state from an adjacent state, only one power switch changes between on and off. The device stress in switching devices of H-bridge circuit is higher than that in SC circuit. It can also be found that the output voltage in Mode 1 is more stable than Mode 2 due to less discharging period of switching capacitor. Along with the up-down movement of modulation signals (Vm 1c, Vm 1b, Vm 2c, Vm 2b), the output voltage of the proposed inverter is a controllable nine-level staircase. The duration of each voltage level is determined by the duty-cycle of SC circuit and the phase-shifted angle of H-Bridge circuit.

Table.1 Relations of on-state switches and output voltage

Mode 1			Mode 2		
On-state switches	Output voltage	Capacitor State	On-state switches	Output voltage	Capacitor State
$S_{1a}, S_{1c}, S_{2a}, S_{2c}, S_1, S_2$	$4V_{in}$	C_1, C_2 Discharging	$S_{1a}, S_{1c}, S_{2a}, S_{2c}, S_1, S_2$	$4V_{in}$	C_1, C_2 Discharging
$S_{1a}, S_{1c}, S_{2a}, S_{2c}, S_1', S_2$	$3V_{in}$	C_2 Discharging	$S_{1a}, S_{1c}, S_{2a}, S_{2c}, S_1', S_2$	$3V_{in}$	C_2 Discharging
$S_{1a}, S_{1c}, S_{2a}, S_{2c}, S_1' S_2'$	$2V_{in}$	C_1, C_2 Charging	$S_{1a}, S_{1b}, S_{2a}, S_{2c}, S_1' S_2$	$2V_{in}$	C_2 Discharging
$S_{1a}, S_{1b}, S_{2a}, S_{2c}, S_1' S_2'$	V_{in}	C_1, C_2 Charging	$S_{1a}, S_{1b}, S_{2a}, S_{2c}, S_1' S_2'$	V_{in}	C_1, C_2 Charging
$S_{1a}, S_{1b}, S_{2a}, S_{2b}, S_1' S_2'$ or $S_{1c}, S_{1d}, S_{2c}, S_{2d}$	0	C_1, C_2 Charging	$S_{1a}, S_{1b}, S_{2a}, S_{2b}, S_1' S_2'$ or $S_{1c}, S_{1d}, S_{2c}, S_{2d}$	0	C_1, C_2 Charging
$S_{1c}, S_{1d}, S_{2b}, S_{2d}, S_1' S_2'$	$-V_{in}$	C_1, C_2 Charging	$S_{1c}, S_{1d}, S_{2b}, S_{2d}, S_1' S_2'$	$-V_{in}$	C_1, C_2 Charging
$S_{1b}, S_{1d}, S_{2b}, S_{2d}, S_1' S_2'$	$-2V_{in}$	C_1, C_2 Charging	$S_{1c}, S_{1d}, S_{2b}, S_{2d}, S_1' S_2$	$-2V_{in}$	C_2 Discharging
$S_{1b}, S_{1d}, S_{2b}, S_{2d}, S_1', S_2$	$-3V_{in}$	C_2 Discharging	$S_{1b}, S_{1d}, S_{2b}, S_{2d}, S_1', S_2$	$-3V_{in}$	C_2 Discharging
$S_{1b}, S_{1d}, S_{2b}, S_{2d}, S_1, S_2$	$-4V_{in}$	C_1, C_2 Discharging	$S_{1b}, S_{1d}, S_{2b}, S_{2d}, S_1, S_2$	$-4V_{in}$	C_1, C_2 Discharging

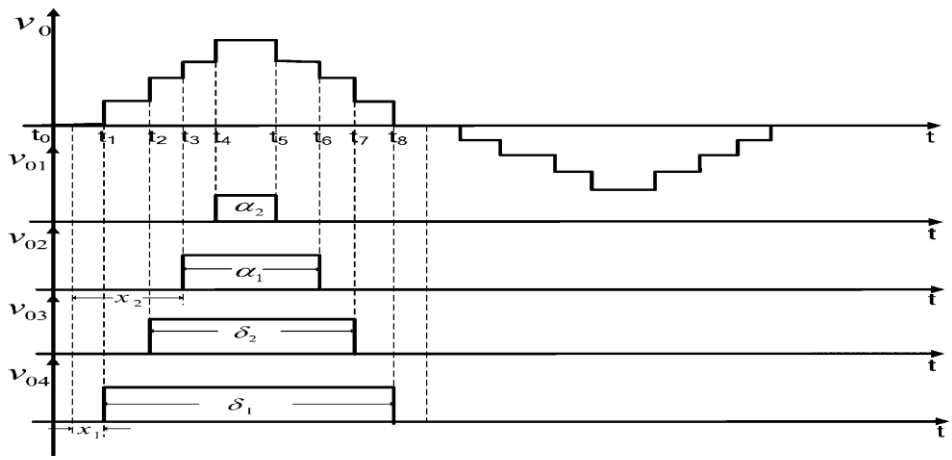

Fig. 3. Output voltage decomposition for Fourier analysis in mode 1.

The numerical benchmark and THD optimization will be examined in the future study, and a fixed ratio ($k1 = k2 = 0.5$, $x1 = \pi/8$, $x2 = \pi/4$) is adopted to evaluate output harmonics in subsequent simulation and experiment. If the proposed dc–ac inverter is used as second stage of ac–ac conversion, an ac–dc controlled rectifier is introduced a preceding stage of ac–ac conversion. Power factor correction (PFC) implemented by dc–dc converter can improve the power factor in ac–dc conversion. In this case, both SC and H-bridge generate the optimized pulse width to minimize output THD. The magnitude regulation of output voltage can be performed by controllable ac–dc stage in input side. The minimized THD is achieved by this two- stage power circuit, namely, ac–dc stage is used to regulate magnitude, and dc–ac stage formed by the proposed inverter is used to minimize THD.

Table.2 Components Comparison Of Proposed Inverter And Cascaded H-Bridge:

Inverter type	Proposed inverter enhanced by SC n×2 topology	Proposed inverter enhanced by H-Bridge 2×n topology	Cascaded H-Bridge
Switching device	2n+8	6n	8n
Capacitor	2n-2	n	0
Diode	4n-6	n	0
DC bus	2	n	2n
Power losses	$(2n-2)loss_{cap}+(4n-6)loss_{diode}+(2n+8)loss_{switch}$	$nloss_{cap}+nloss_{diode}+6nloss_{switch}$	$8nloss_{switch}$

An $n \times 2$ topology needs $2n - 2$ capacitors, $2n + 8$ switches, and 2 dc inputs; $2\times n$ topology needs n capacitors, $6n$ switches, and n dc inputs. The traditional cascaded H-Bridge needs $8n$ switches and $2n$ dc inputs. With the same number of voltage levels, the proposed inverter needs less switching devices and inputs than the traditional cascaded H-Bridge. The fundamental frequency is 25 kHz that is the same as output frequency. It can be observed that the fundamental harmonic is significantly higher than the other harmonics. The magnitude of fundamental component is below 40 V for nine-level inverter.The calculated THD is 19.1% for 9-level inverter .It can be estimated that the harmonics can be further cut down along with the increasing number of voltage levels. Thus, the proposed inverter produces near sinusoidal staircase output, and two methods can make it more sinusoidal. One is to optimize the duration of voltage levels; the other one is to increase the number of voltage levels.

4. Computer simulation results

Simulink is a software add-on to matlab which is a mathematical tool developed by The Math works,(http://www.mathworks.com) a company based in Natick. Matlab is powered by extensive numerical analysis capability. Simulink is a tool used to visually program a dynamic system (those governed by Differential equations) and look at results. Any logic circuit, or control system for a dynamic system can be built by using standard building blocks available in Simulink Libraries.

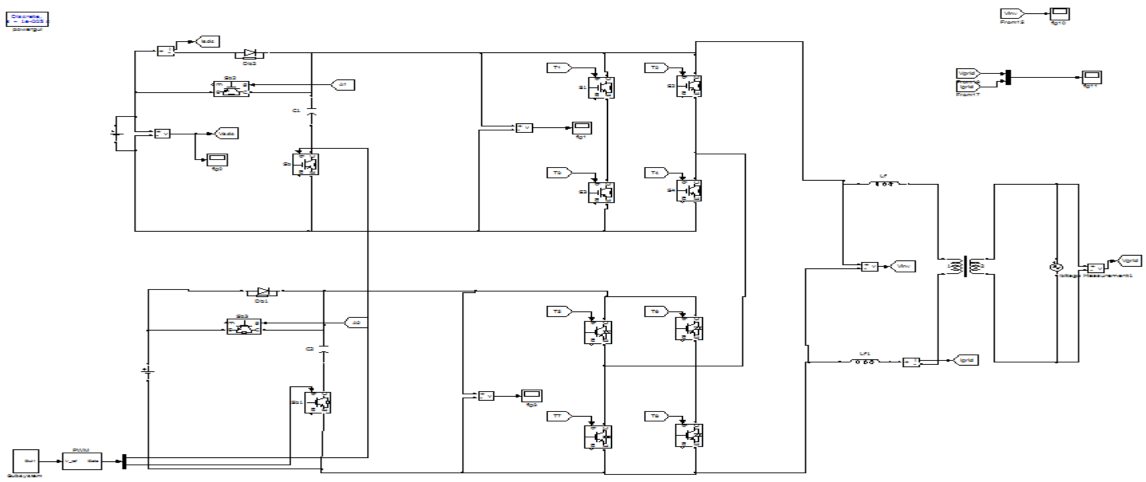

Fig.4 simulation circuit of nine level inverter

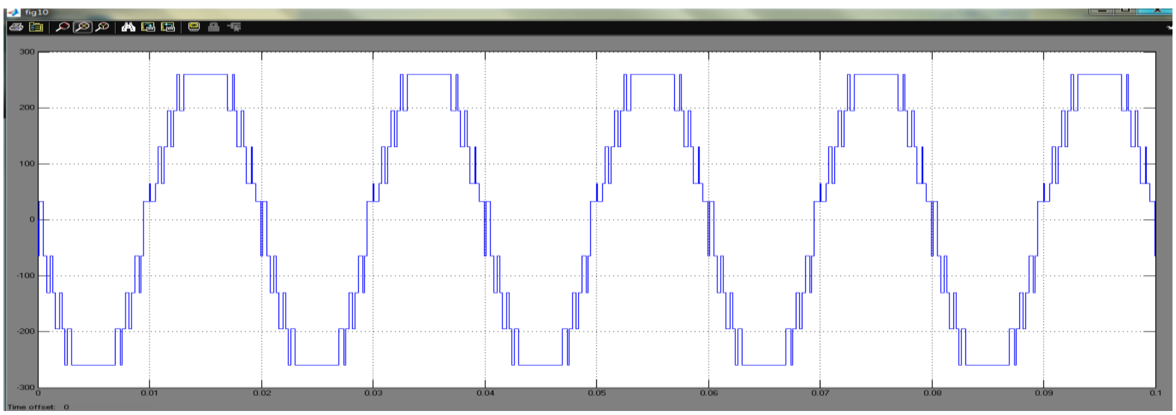

Fig 5. Nine level inverter output voltage waveform

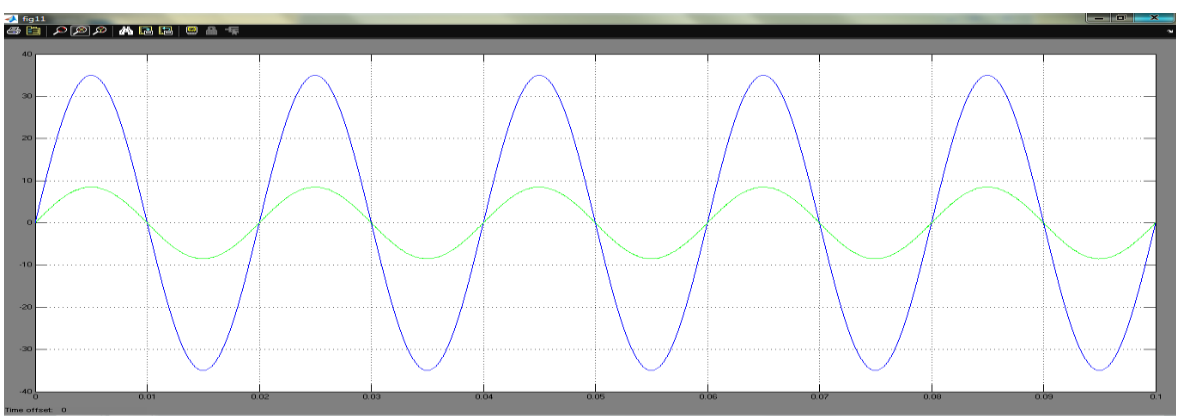

Fig .6. Output voltage and current waveforms at Grid

5.Conclusion

In this proposed work, a switched capacitor based cascaded multilevel inverter with reduced total harmonic component was proposed. The nine level output compared with conventional cascaded multilevel inverter, the proposed inverter can decrease the number of switching components. A single carrier modulation technique with the low switching frequency was presented. The simulation results obtained confirms the feasibility of proposed circuit and modulation method. Comparing with cascade H-bridge, the number of voltage levels can be further increased by this method. The number of voltage levels increases two times in half cycle of nine level converter output. With the increase in the number of voltage levels, the harmonics are significantly reduced in the staircase output. Meanwhile, the magnitude control can be achieved by pulse width regulation of voltage level, so the proposed multilevel inverter can serve as HF power source with controlled magnitude and lesser harmonics. In this proposed work the nine level inverter was analyzed. The proposed inverter can be applied to grid-connected photovoltaic system and electrical network of EV, because the multiple dc sources are available easily from solar panel, batteries ,Ultra capacitors, and fuel cells.

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