Low Power High Speed Low Offset Regenerative Comparator

Swati Singh, M.Tech. Student, DIMAT , Pankaj Gulhane, Asst professor, DIMAT,

Abstract – In high speed ADC, a comparator directly influence the overall performance of ADC. In his paper we are reviewing different techniques for designing of comparators used in analog-to-digital converters. Following is a review for different techniques of low offset, high speed and regenerative type of preamplifier and latch structure. Two stages (preamplifier and latch) of comparator is provide a high speed which can then be implemented for low offset , high gain ,low threshold and low power. This implementation gives a high performance of a comparator. We are presenting details analysis of different techniques in this.

Index Terms: - Analog-to-Digital Converter, comparator,

Digital logic, CMOS, latch.

I. INTRODUCTION

Comparators are fundamental building block for Analog-to-Digital converters and regulators. ADC's are used in many applications such as data storage systems, fast serial links, high speed communication and interfaces, which required for high resolution and high speed of the order of GSPS. In many applications comparator is a key element for conversion therefore widely used in circuit design. Basically it compares two analog inputs and gives a logical value at the output which depends on polarity of the input voltage different. Power consumption and speed are very important factors in comparator design. Low power consumption is very demanding for today's technology because it increases the battery lifetime. There have been many researches focusing on lowering the power consumption and using different techniques.

Architecture of a high speed comparator essentially consists of a preamplifier stage and a latching stage. In the pre-amplification stage the difference between the input signals is amplified thus the output voltage difference tracks the input signal. In the latching stage the output of amplification go through a digital logic level. This high speed comparator is further modified for increasing the performance of comparator.

This paper introduces a number of comparator design techniques for the use of ADC's. The techniques are used to improve different performance parameters

II. DIFFERENT TECHNIQUE FOR COMPARATOR DESIGNING

There has been a growing demand for the development of low power circuit. Thus many researchers are trying to reduce the power consumption of any circuit. In this paper some different techniques are describing for low power comparators.

A. A REGENERATIVE COMPARATOR STRUCTURE WITH INTEGRATED INDUCTORS

A regenerative comparator structure with integrated inductors uses an inductor for improving the power consumption and sampling speed of comparator. Power consumption and sampling speed are two most important factors for comparator design. Sampling speed and power consumption of comparators improves as the transistor gate length is increased. Mostly comparators having two components: first a preamplifier and second a regenerative latch. Figure 1 shows the basic block diagram of comparator in which the combination of a transconductance and a load resistance represents a pre-amplifier and the combination of negative resistance and a load resistance represents a latch.

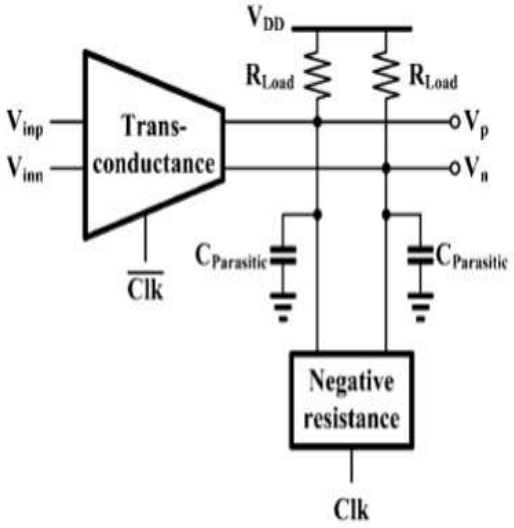

Figure 1

The operation of the comparator is controlled by the complementary clocks Clk and Clk'. When Clk is low, the comparator is in tracking mode and in this mode the latch is disabled, and the transconductance of preamplifier is enabled. The difference between input signals is amplified thus output voltage difference tracks the input signals. When Clk goes high latch is enabled and due to a negative resistance a regenerative circuit is formed which amplifies V_p and V_n to a digital logic level.

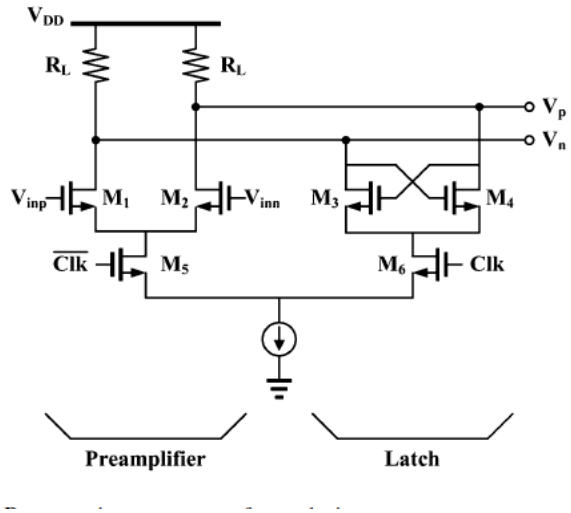

Figure 2

Figure 2 shows the circuit diagram for a regenerative comparator in which transistor $M_{1\text{-}2}$ provide the transconductance for preamplifier and transistor $M_{3\text{-}4}$ as cross coupled generate negative resistance for the latch. In the pre-amplification kick back noise reduces and also the offset of the latch reduces by the gain of the amplifier.

Implementation in Comparator Structure:

By the addition of inductor bandwidth in the pre-amplification stage is increased and the regenerative time constant decreased thus with the help of inductor both the tracking and latching speed is increased. The probability decreases exponentially with reduction in the regenerative time constant. Inductor is added to improve the performance of comparator. The inductor is connected in series with the load resistor. A large inductor parasitic is managed if the parasitic resistance is considered as a part of load resistor. The use of thinner metal lines in the inductor is beneficial for comparator.

B. A NOVEL 1GSPS LOW OFFSET COMPARATOR FOR HIGH SPEED ADC

This paper describes a low power and ultra high speed low offset preamplifier-latch comparator. There have many types of comparators which provide high speed but the speed more than 1GSPS is hardly achieved because of the limitation of the bandwidth of amplifier. The dynamic latch comparator is used for high speed. In this comparator two negative resistances in parallel to load resistance are used. The comparator uses novel method to reduce the recovery time. This paper based on the analysis of the speed and offset of preamplifier-latch comparator.

Basic Operation:

The proposed comparator of this paper consists of a preamplifier, regenerative latch and output latch. The input signals delivered to preamplifier which reduces the offset voltage. The regenerative latch compares the inputs and the output latch integrates the final output. The Clk signal is used in the regenerative mode to reduce the power consumption caused by the dynamic current of the transistor. The final output is generated by the the output latch.

Effected Parameters:

In high speed comparators at the preamplifiers stage the bandwidth is high thus the gain is also high to amplify the input signals. The proposed comparator the offset is caused by the preamplifier thus the offset voltage is reduced. The propagation delay of this paper is also reduces due to the channel length. Thus these parameters are changed for improved performance of the comparator.

C. A 0.35MM CMOS COMPARATOR CIRCUIT FOR HIGH-SPEED ADC APPLICATIONS

This paper presents a high speed differential clocked comparator circuit. The comparator circuit consists of a pre-amplifier and a latch stage with the dynamic latch at the output. At the output the circuit consists of a full transmission gate (TG) and two inverters which help in the reduction of power consumption.

Basic Blocks Diagram of Proposed Comparator:

The block diagram of the comparator is shown in figure 3 which consists of three main blocks a pre-amplifier, a latch and an output sampler. Transmission gate and inverter is used in output sampler and the combination of both acts as a holding capacitor. The outputs are sampled at the end of evaluation phase. The samples are amplified using the output inverters.

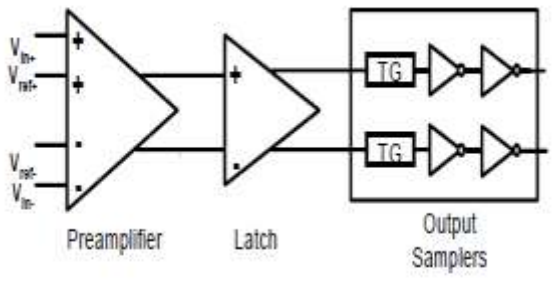

Figure 3

Implementation due to Transmission Gate

When a TG is used as a sampling switch, charge injection is occurs which creates some problems with the operation of the circuit. However in the proposed comparator architecture, voltage changes due to the charge injection and adds to the sampled signals.

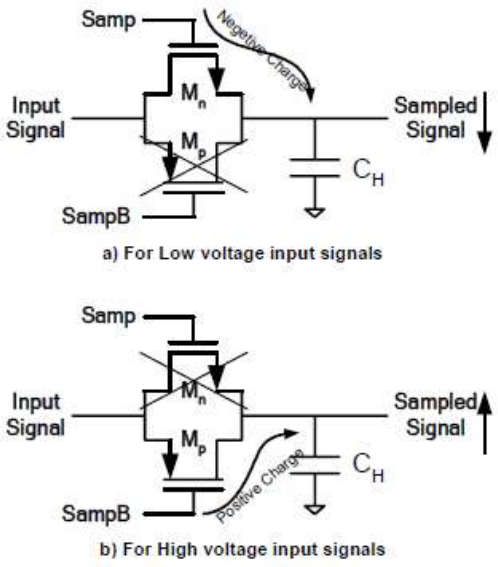

Figure 4

Figure 4 shows the effect of charge injection in TG, when TG is in track mode, ''samp" is high and M_n transistor acts as closed switch for low input voltages. At the end of track mode "samp" changes to low and the M_n switch is opened. Thus the charge injection changes the voltage level.

III. CONCLUSION

There are different techniques are used for improving the performance of a comparator. By the addition of an inductor the load resistance is decreases thus the latching speed is increased. The technique become more beneficial with the smaller inductance as the gate length shrink. This technique is applicable to all type of comparators. In the novel method for high speed the comparator uses two negative resistors parallel with positive resistors as the load resistors of preamplifier to improve its gain thus the offset voltage is reduced. It is suitable for 1GSPS high speed ADC. By using a TG at the output sampler stage the power consumption of comparator is reduces. Also TG's charge injection enhances the voltage level of sampled signals.

REFERENCES:

1. Behzad Razavi, Beuce A.Wooley,"Design Techniques for High Speed, High-Resolution Comparators",
2. Sunghyun Park, Michael P. Flynn,"A regenerative Comparator structure with Integrated Inductors",IEEE Transaction on Circuits and Systems- I VOL.-53, NO. 6, AUGUEST 2006.
3. Ali Valaee, Mohammadi Maymandi-nejad and Vakilabad BLVD Mashhad, "An Ultra Low-Power Low- Voltage Track and latch Comparator", IEEE ICECS 2010.
4. Meena Panchor and R. S. GAMAD, "Low Power High Speed CMOS Comparator design using 0.18 µm Technology", ISSN 0975-6450 VOL- 2 NO. 1 (2010) pp 71-77
5. Guo Yongheng , Cai Wei, Lu Tiejun, Wang Zongmin, "ANovel 1GSPS Low Offset Comparator for High Speed ADC", IEEE computer society 2009
6. Samad Sheikhaei, Shahriar Mirabbasi, and Andre Ivanov" A 0.35µm CMOS Comparator Circuit for High Speed ADC Applications",IEEE NSERC 2005
7. Khayrollah Hadidi and Gabor C. Temes, "A High Resolution Low Offset and High Speed Comparator", IEEE 1992 CUSOM INTEGRATED CIRCUITS CONFERENCE
8. Benjamin J. McCarroll, CharlEs G. Sodini Hea Seung Lee, "A High Speed CMOS Comparator for Use in an ADC", IEEE JOURNALS OF SOLID STATE CIRCUITS VOL 23, NO 1, Feb1988
9. P. E. Allen, and D.R. Holberg "CMOS Analog Circuit Design" Second addition Oxford university 2007
10. R JACOB BAKER"CMOS Circuit design and layout and simulation", IEEE PRESS second edition